DLC Display Co., Limited

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Record of Revision

Date	Revision No.	Summary
2020-10-18	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0283BEM04DB-R-3 active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC, Resistive touch panel and a backlight unit. The 2.8” display area contains 240(RGB) x 320 pixels.

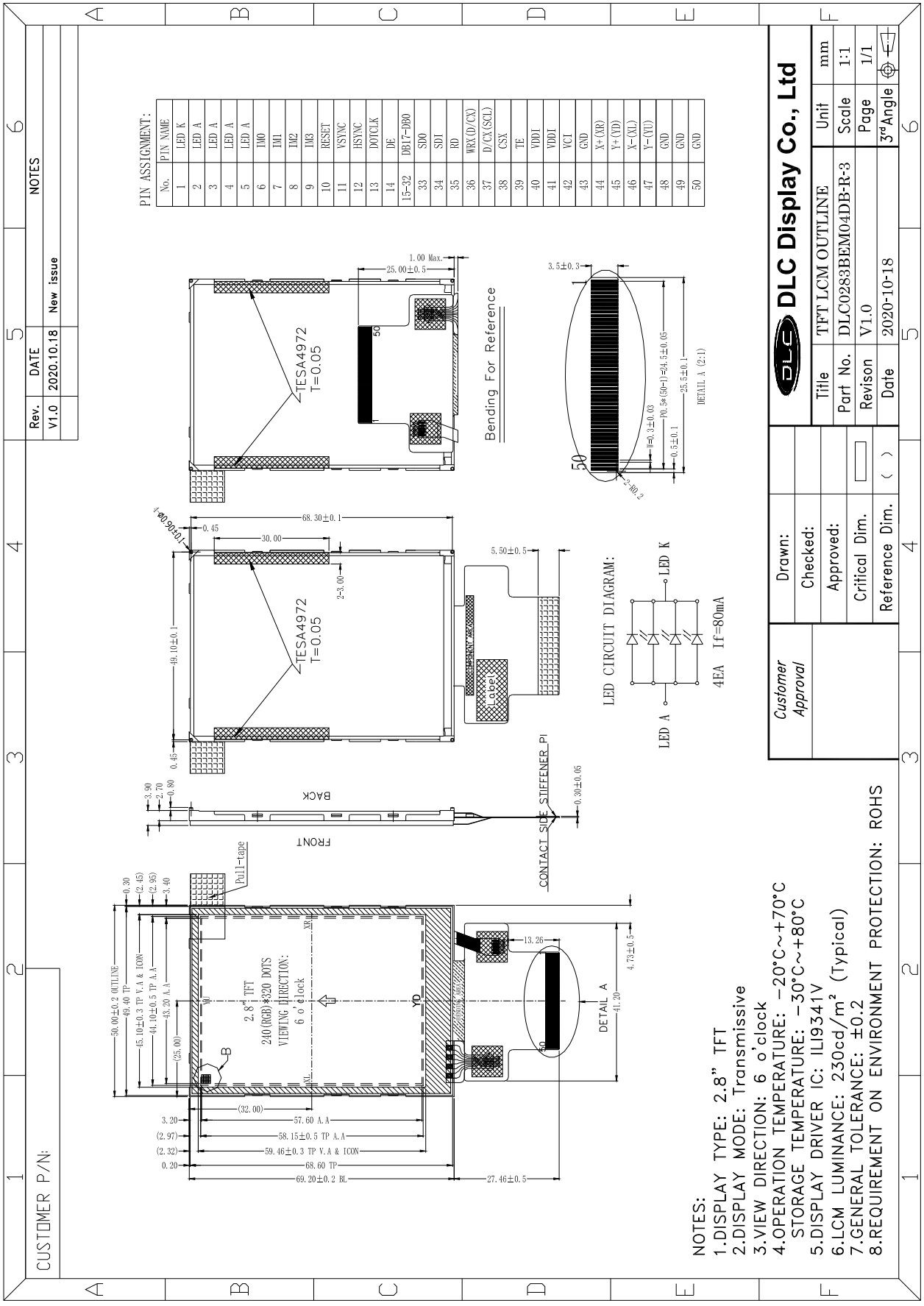
2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	2.8	inch
Resolution	240(RGB) x 320	/
Interface	RGB	/
Technology type	a-Si TFT	/
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	50.00 x 69.20 x 3.90	mm
Active Area	43.20 x 57.60	mm
Display Mode	Transmissive	/
Backlight Type	LED	/
Driver IC	ILI9341V	/
Viewing Direction	6 o’clock	/

4. Outline Drawing



5. Interface signals

Pin No.	Symbol	Function
1	LED-K	LED Backlight Cathode
2~5	LED-A	LED Backlight Anode
6	IM0	Select the interface Note 1
7	IM1	Select the interface Note 1
8	IM2	Select the interface Note 1
9	IM3	Select the interface Note 1
10	RESET	Reset signal
11	VSYNC	Frame signal for interface operation
12	HSYNC	Line signal for interface operation
13	DOTCLK	Dot clock signal
14	DE	Data enable signal
15~32	DB17-DB0	Data input
33	SDO	Serial output signal
34	SDI	Serial input signal
35	RD	Read signal
36	WRX(D/CX)	Write signal
37	(D/CX)SCL	The serial interface clock
38	CSX	Chip select input pin
39	TE	Effect output pin to frame writing
40~41	VDDI	Digital I/O pad power supply
42	VCI	Power supply for logic
43	GND	Ground
44	X+ (XR)	Touch panel control pin
45	Y+ (YD)	Touch panel control pin
46	X- (XL)	Touch panel control pin
47	Y- (YU)	Touch panel control pin
48~50	GND	Ground

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	VCI	-0.3	3.6	V	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. VCC >VSS must be maintained.

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

Note:

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.
   The phenomenon is reversible.
3. Ta<=40℃:85%RH MAX.
   Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

7. Electrical Specifications

7.1 Electrical characteristics

VSS=0V, Ta=25℃

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note	Condition
Power Supply		VCI	2.6	2.8	3.3	V		Ta=25℃
Input Voltage	“H”	VIH	0.8*VCI	-	VCI	V		VCI=2.8V
	“L”	VIL	0	-	0.2*VCI	V		VCI=2.8V
Current Consumption		I_{DD1}	-	10	15	mA	Note 1	Normal mode
		I_{DD2}	-	0.05	0.1	mA	Note 1	Sleep mode

Note: Tested in 1x1 chessboard pattern.

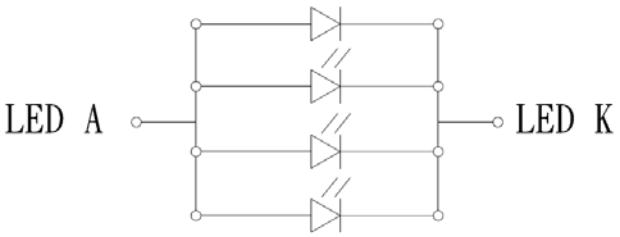
7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	80	-	mA	
Forward Voltage	VF	-	3.0	-	V	
LED life time	--	-	30,000	--	Hr	Note

Note: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL =80mA. The LED lifetime could be decreased if operating IL is larger than 80mA.

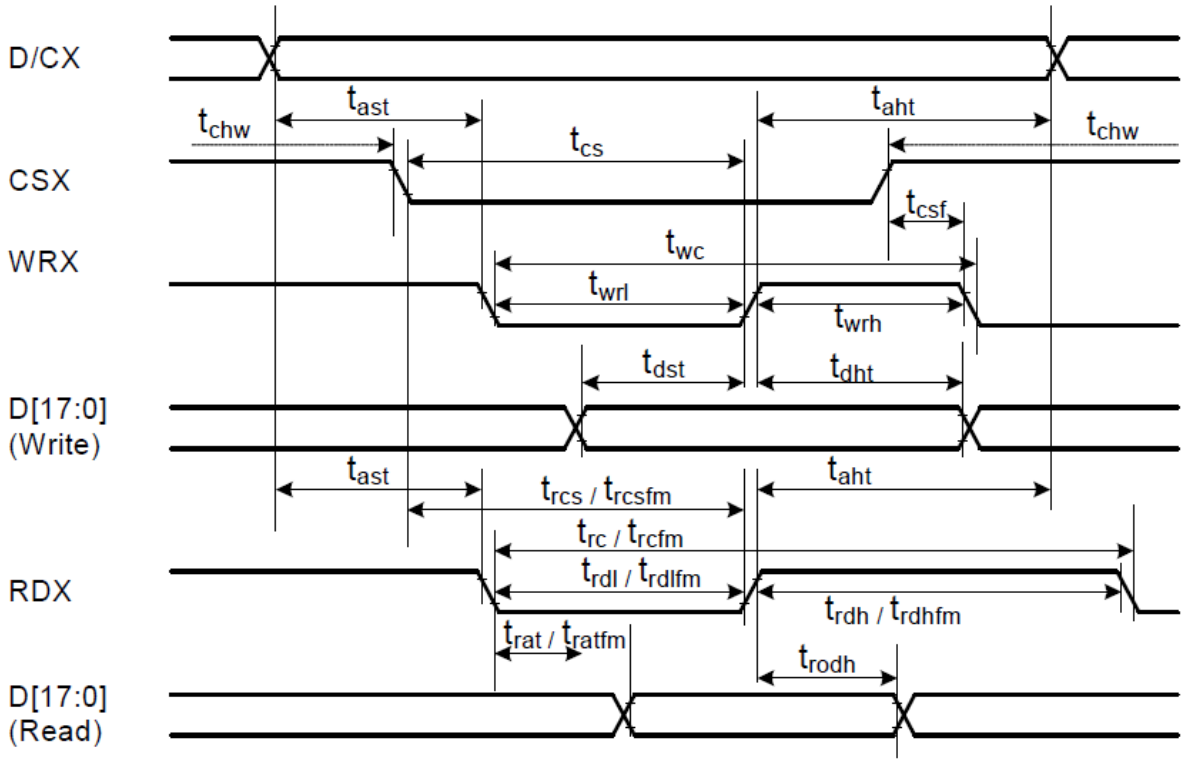
LED CIRCUIT DIAGRAM:



4EA If=80mA

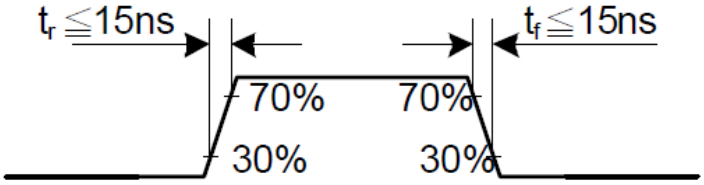
8. Command/AC Timing

8.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

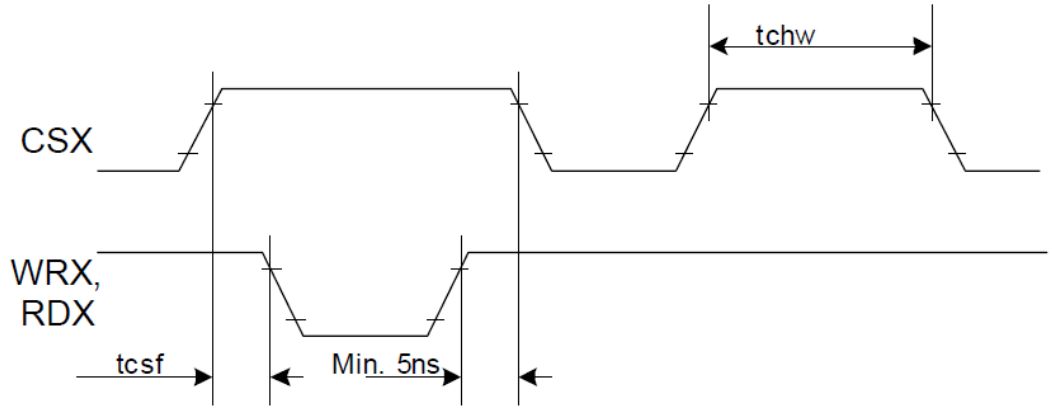


Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (write/read)	0	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip select setup time (write)	15	-	ns	
	trcs	Chip select setup time (read ID)	45	-	ns	
	trcsfm	Chip select setup time (read FM)	355	-	ns	
	tcsf	Chip select wait time (write/read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write control pulse H duration	15	-	ns	
	twrl	Write control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read control H duration (FM)	90	-	ns	
	trdlfm	Read control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read control pulse H duration	90	-	ns	
	trdl	Read control pulse L duration	45	-	ns	
D[17:0] D[15:0] D[8:0] D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta= -30 to 70℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, VSS= 0V.

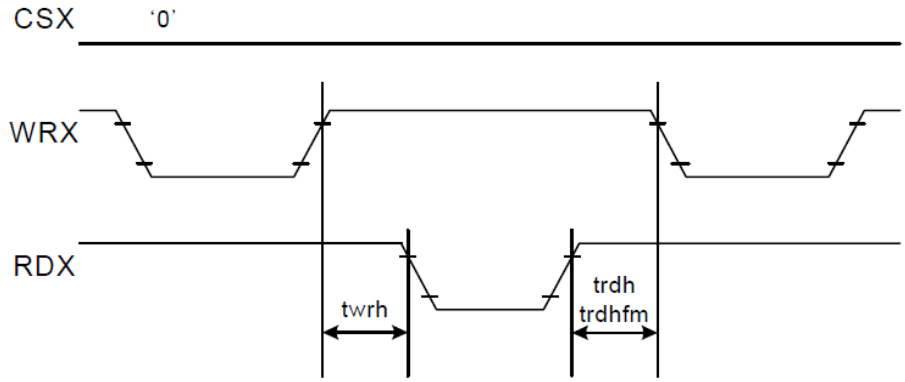


CSX Timings:



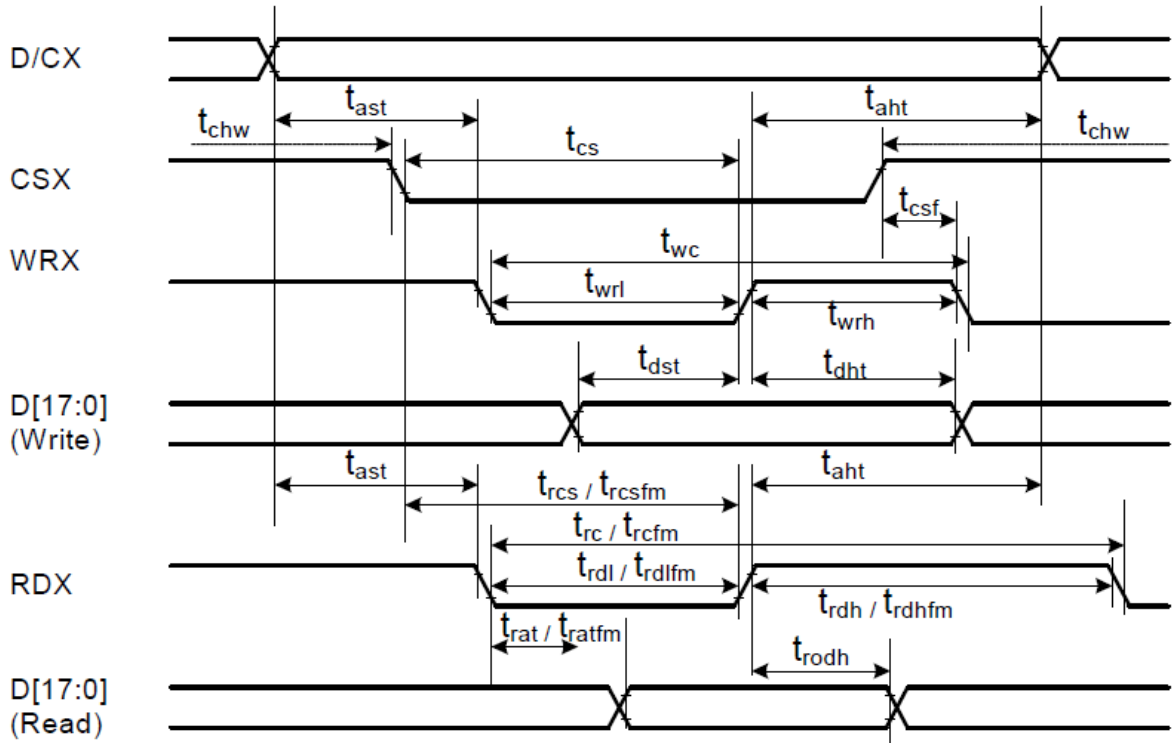
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

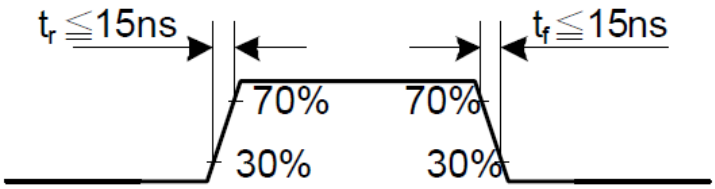
8.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)



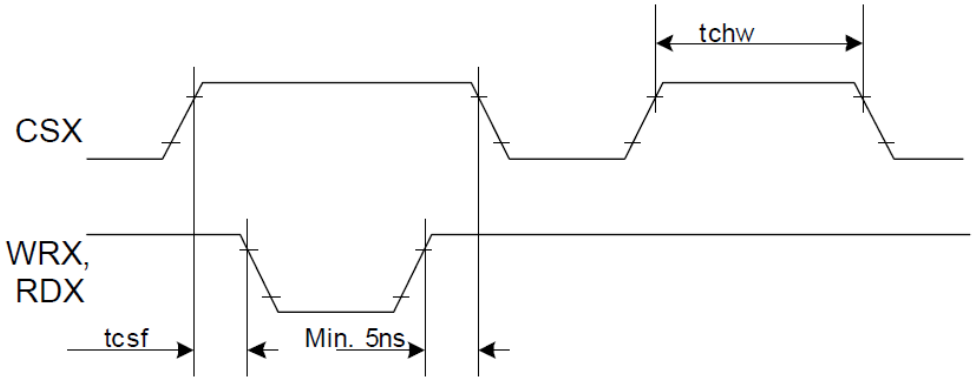
Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (write/read)	0	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip select setup time (write)	15	-	ns	
	trcs	Chip select setup time (read ID)	45	-	ns	
	trcsfm	Chip select setup time (read FM)	355	-	ns	
	tcsf	Chip select wait time (write/read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write control pulse H duration	15	-	ns	
	twrl	Write control pulse L duration	15	-	ns	
RDX	trcfm	Read cycle (FM)	450	-	ns	

(FM)	trdhfm	Read control H duration (FM)	90	-	ns	
	trdlfm	Read control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read control pulse H duration	90	-	ns	
	trdl	Read control pulse L duration	45	-	ns	
D[17:0] D[17:10] &D[8:1] D[17:10] D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta= -30 to 70℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, VSS= 0V.

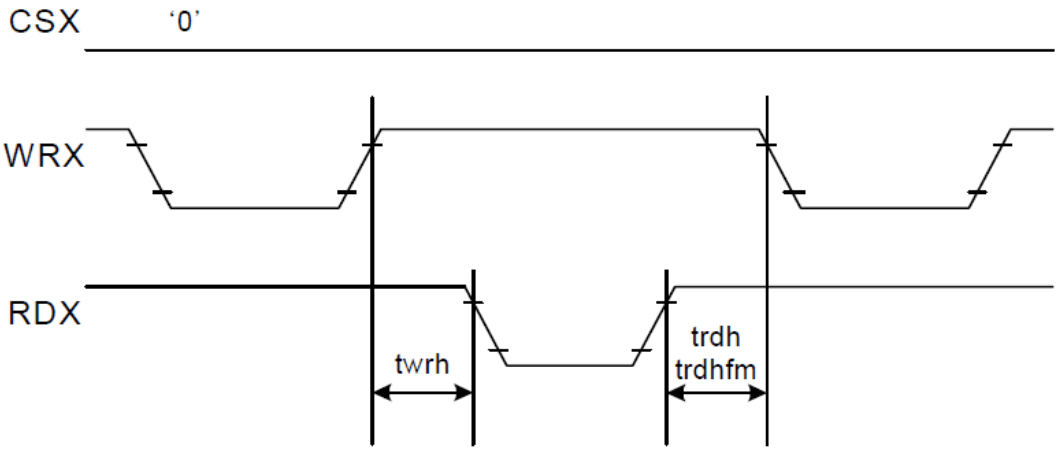


CSX timings:



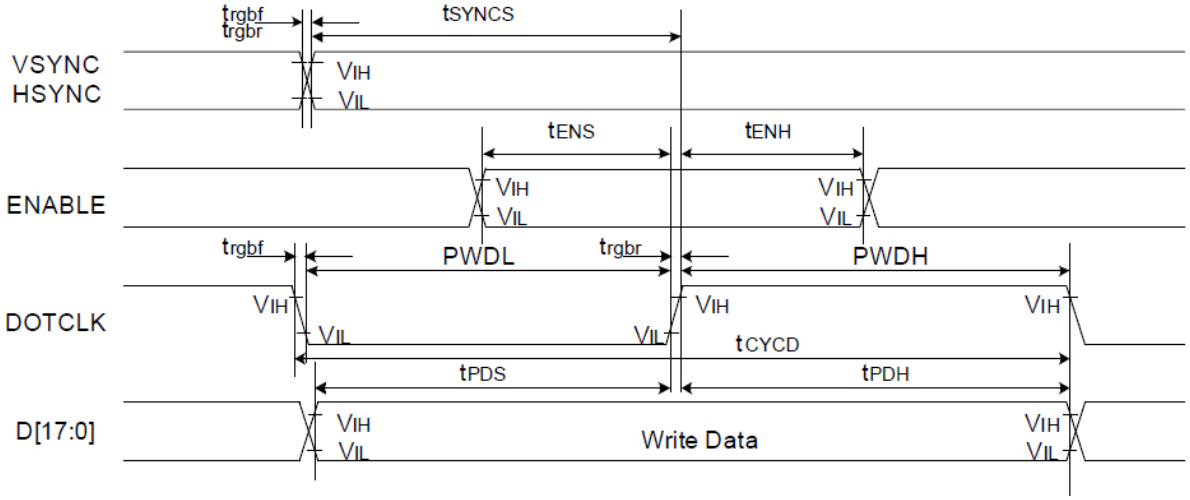
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



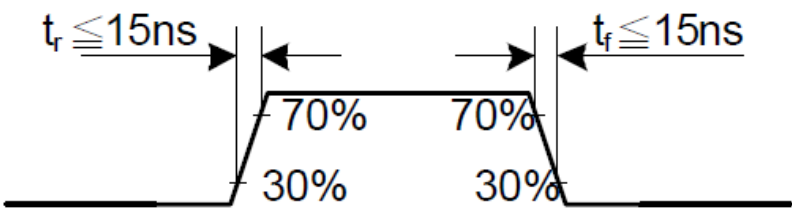
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC/ HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-		18/16-bit bus RGB Interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-		
DE	tENS	DE setup time	15	-		
	tENH	DE hold time	15	-		
D[17:0]	tPOS	Data setup time	15	-		
	tPDH	Data hold time	15	-		
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	100	-		
	trgbr, trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15		
VSYNC/ HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB Interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
DE	tENS	DE setup time	15	-	ns	
	tENH	DE hold time	15	-	ns	
D[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	50	-	ns	
	trgbr, trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta= -30 to 70℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, AGND=VSS= 0V.



5.2 Reset Timings

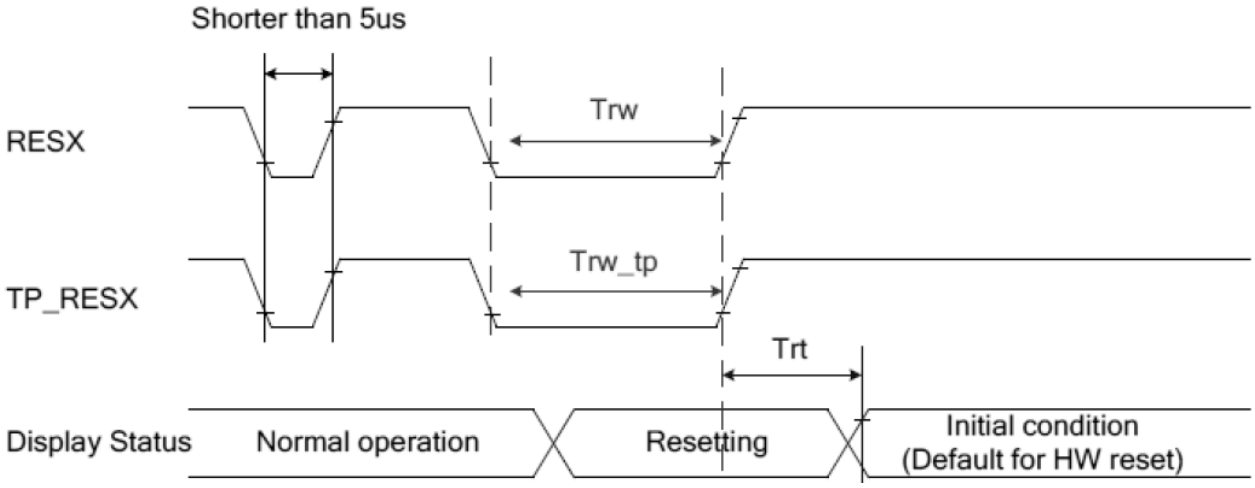


Figure: Reset Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	Trw	Reset pulse duration	10	-	us
	Trt	Reset cancel	35(Note1,5)	-	ms
			150(Note1,6,7)	-	ms
TP_RESX	Trt_tp	Reset pulse duration	1	-	us

Table: Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other setting from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts in sleep out mode. The display remains the blank state in sleep in mode.) and return to default condition for hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

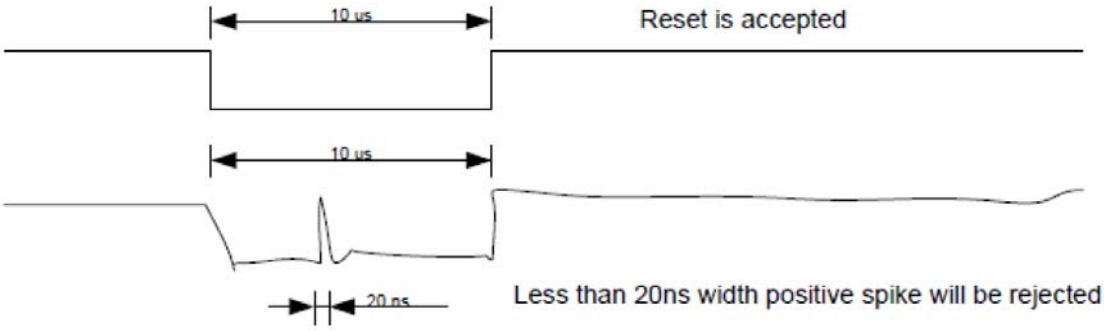


Figure: Positive Noise Pulse during Reset Low

5. When Reset applied during sleep in mode.
6. When Reset applied during sleep out mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also sleep out command (11h) cannot be sent for 120msec.

9. Optical Specification

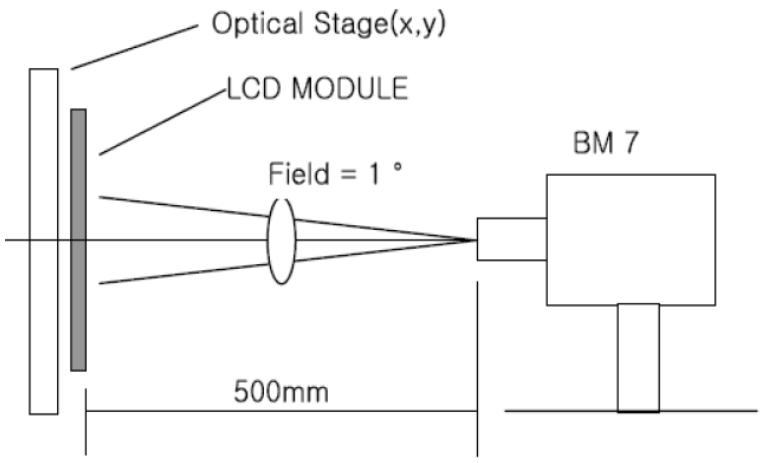
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	300	500	-		Note1 Note2
Response Time		Tr	25℃	-	10	-	ms	Note1 Note3
		Tf			10	-	ms	
View Angles		θT	CR≧10	-	65	-	Degree	Note 4
		θB		-	55	-		
		θL		-	65	-		
		θR		-	65	-		
Chromaticity	White	x	Brightness is on	Typ-0.05	0.28	Typ+0.05		Note5, Note1
		y			0.33			
	Red	x			0.51			
		y			0.34			
	Green	x			0.31			
		y			0.56			
	Blue	x			0.15			
		y			0.14			
NTSC		S		50	60	--	%	Note5
Luminance		L		-	230	-	cd/m^2	Note1 Note6
Uniformity		U		80	-	-	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃);

LED back-light: ON, Environment brightness < 150 lx

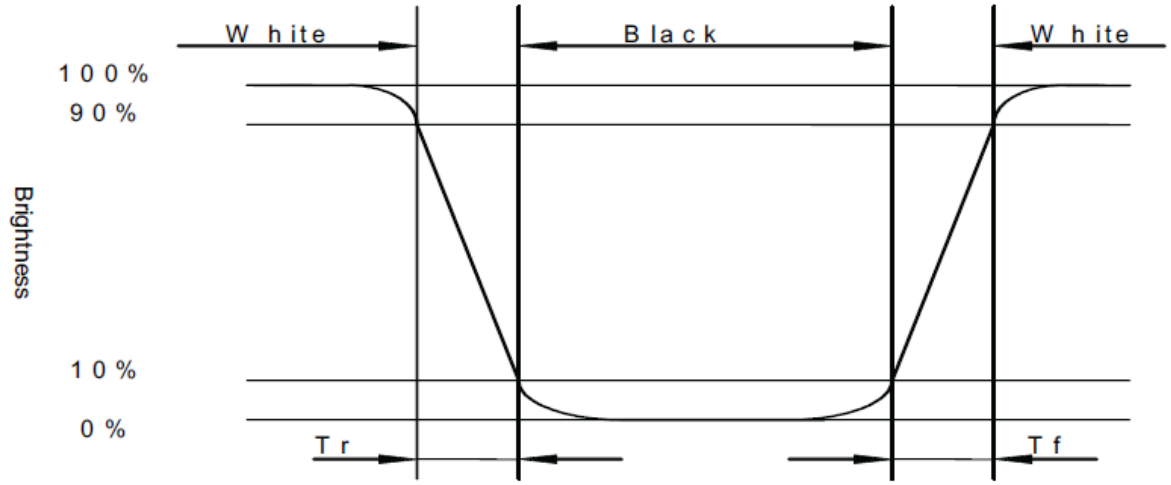


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

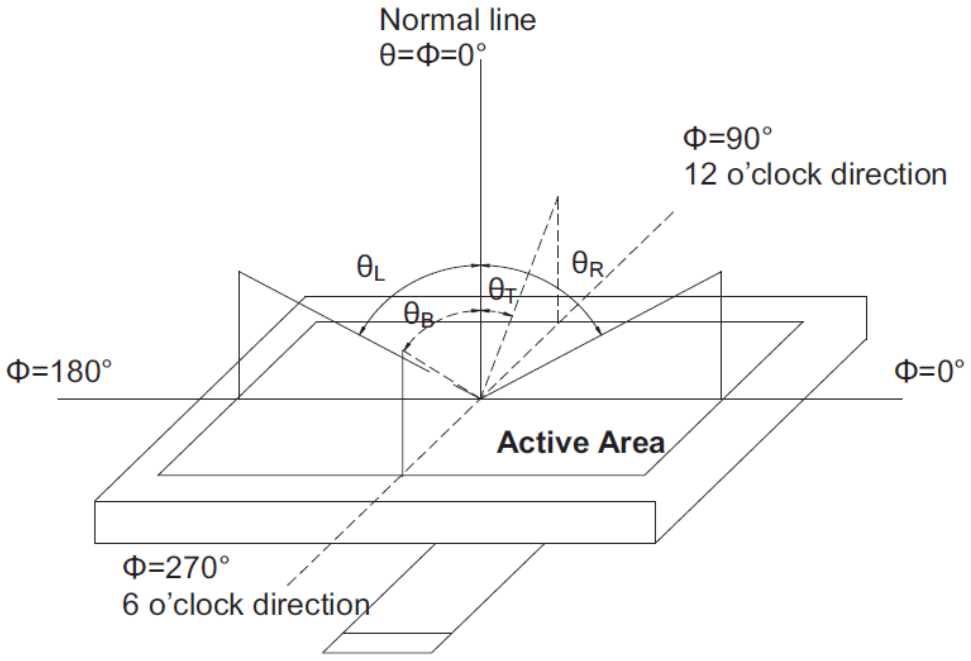
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



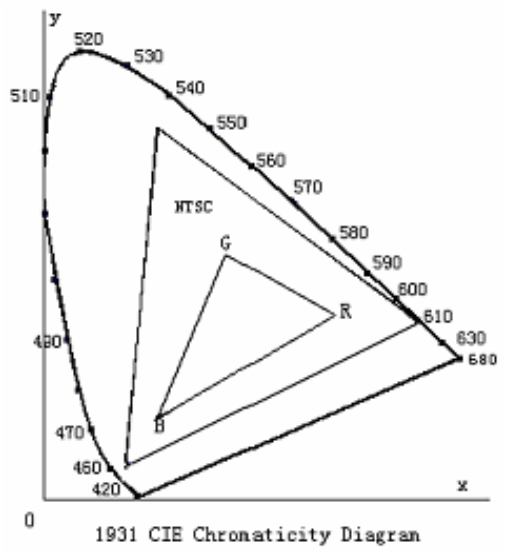
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

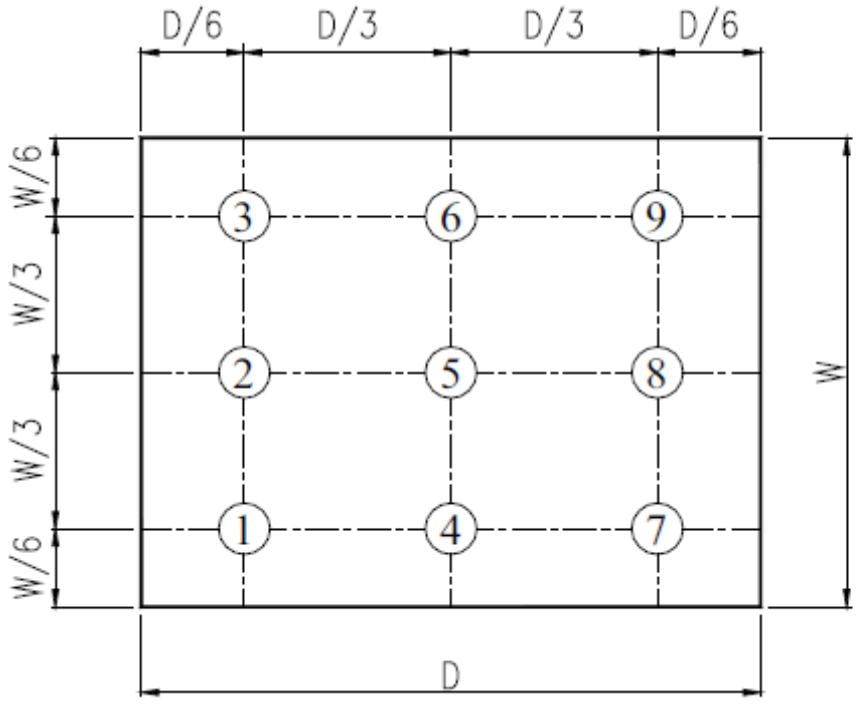


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta=+70℃, 96hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 96hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 96hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 96hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+80℃ 30 min, Change time:5min, 5 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	10Hz~150Hz, 100m/s2, 120min	Per table in below
9	Shock (Non-operation)	Half- sine wave,300m/s2,11ms	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

10.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

10.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

10.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

10.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

10.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

10.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, DLC recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.